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Zilka-Kotab, PC
P.O. BOX 721120
SAN JOSE, CA 95172-1120

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ELAND, SHAWN	

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dottie@zilkakotab.com
jennifer@zilkakotab.com

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MICHAEL C. STOLOWITZ

Appeal 2009-005678
Application 10/822,115[1]
Technology Center 2100

Decided: December 17, 2009

Before JEAN R. HOMERE, JAY P. LUCAS, and DEBRA K. STEPHENS, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Application filed April 8, 2004. Appellant claims the benefit under 35 U.S.C. § 119 of provisional application 60/461,445, filed April 9, 2003. The real party in interest is NVIDIA Corporation.

STATEMENT OF THE CASE

Appellant appeals from a final rejection of claims 1-31 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b).

Appellant's invention relates to a method for transferring read data from an array of independent disk drives (claim 1). In the words of Appellant:

> [A]fter issuing read commands to all of the drives, we wait until there is data available for transfer in all of the FIFOs, i.e. that they are all indicating a "not empty" condition. . . . After an indication that all FIFOs have data; i.e., all of the FIFOs have data from their corresponding drives, the read data is transferred.

(Spec. ¶ [0022]).

Claim 1 is exemplary:

> 1. A method of reading stored data from an array of independent disk drives so as to provide synchronous data transfer into a buffer, the method comprising:
>
> for each disk drive in the array, providing a corresponding two-port memory for receiving and storing read data responsive to timing signals provided by the respective drive;
>
> initiating a READ command to each of the drives of the array, thereby causing each of the drives to retrieve selected elements of its stored data, and to transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive;

> monitoring each of the two-port memories to detect a non-empty condition;
>
> waiting until all of the two-port memories indicate such a non-empty condition;
>
> then synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer; and
>
> repeating said monitoring, waiting; [sic] reading and writing into the buffer steps until completion of a read operation initiated by the said READ command.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Searby	US 5,765,186	Jun. 09, 1998
Yamamoto	US 5,801,859	Sep. 01, 1998
Stolowitz	US 6,018,778	Jan. 25, 2000
Anderson	US 2003/0200478 A1	Oct. 23, 2003

REJECTIONS

The Examiner rejects the claims as follows:

R1: Claims 1, 3-5, 8, 10-12, 14, 16, 26-28, and 31 stand rejected under 35 U.S.C. § 102(b) for being anticipated by Searby.

R2: Claim 15 stands rejected under 35 U.S.C. § 103(a) for being obvious over Searby.

R3: Claims 6, 7, 13, 29, and 30 stand rejected under 35 U.S.C. § 103(a) for being obvious over Searby in view of Anderson.

R4: Claims 2, 9, 17, and 19-25 stand rejected under 35 U.S.C. § 103(a) for being obvious over Searby in view of Stolowitz.

R5: Claim 18 stands rejected under 35 U.S.C. § 103(a) for being obvious over Searby and Stolowitz in view of Yamamoto.

Grouping of Claims:

Claims are addressed in the order of the Examiner's rejections and Appellant's arguments, except as noted below. Claim 1 is representative. *See* 37 C.F.R. § 41.37 (c) (vii).

Appellant contends that the claimed subject matter is not anticipated by Searby, or rendered obvious by Searby alone, or in combination with Anderson, Stolowitz, and/or Yamamoto, because Searby fails to teach "receiving and storing read data responsive to timing signals provided by the respective drive," "monitoring each of the two-port memories," or "synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer," as recited in exemplary claim 1. (*See* App. Br. 13, bottom; App. Br. 17, middle; and App. Br. 18, top.) The Examiner contends that each of the claims is properly rejected (Ans. 28, top).

We affirm the rejections.

ISSUE

The pivotal issue is whether Appellant has shown that the Examiner erred in rejecting the claims under 35 U.S.C. §§ 102(b) and 103(a). Specifically, the issue turns on whether Searby's teachings for simultaneously transferring read data and sequentially writing data to a

buffer read on Appellant's claim limitations "synchronously reading the transferred data from all of the two-port memories" and "writing the synchronous read data into the buffer," (claim 1) respectively.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

Disclosure

1. Appellant has invented a method and apparatus for transferring data from an array of disk drives (claim 1). Signals initiate reads of the disk drives and transfer of read data from the disk drives to two-port memories. (*See id.*) When some read data from the disk drives is transferred into each of the respective memories, the read data is written into the buffer (*id.*).

Searby

2. The Searby reference teaches a data storage apparatus for transferring data from an array of disk stores. (*See* col. 1, ll. 7-8; col. 2, ll. 49-51; col. 6, l. 35; Fig. 2, elements 21-24.) Searby teaches a controller that initiates reads of the disk stores and transfer of read data from each of the stores to corresponding RAM buffers. (*See* col. 5, ll. 38-43.) Searby's signals (*i.e.*, REQs or request signals for read commands) travel between the controller and the disk drives (*see* col. 5, l. 44; Ans. 4, middle), causing each of the drives to transfer read data from the drives into the RAM buffers. (*See* col. 7, ll. 19-23.) The patent says sub-controllers can be substituted for the single controller (*see* col. 7, ll. 11-14) to independently monitor request signals and cause read data to be transferred from the SCSI interfaces of the disk stores to the RAM buffers. (*See* col. 7, ll. 15-

19.) Searby teaches simultaneously reading data from the same location in each of the disc stores and simultaneously transferring the read data from the RAM buffers to the respective registers 41 to 44. (*See* col. 7, ll. 22-23 and 33-39; Fig. 2.) Searby also teaches that read data is written sequentially to the register 50. (*See* col. 7, ll. 46-49; Fig. 2, element 50.)

Anderson

3. The Anderson reference discloses a single-chip storage controller that includes a plurality of storage devices (¶ [0053]; Fig. 2, element 10; Ans. 11, middle).

Stolowitz

4. The Stolowitz reference discloses regenerating or reconstructing user data in the event of a failure of any single drive. (*See* Abstract.)

Yamamoto

5. The Yamamoto reference discloses a network system for plural node devices without arbitration in which the port (either input or output) can be exchanged via multiplexing logic. (*See* col. 30, ll. 3-18; Fig. 24, element 77; Ans. 18, middle.)

PRINCIPLES OF LAW

Appellant has the burden on appeal to the Board to demonstrate error in the Examiner's position. *See In re Kahn*, 441 F.3d 977, 985-86 (Fed. Cir. 2006).

Our reviewing court states in *In re Zletz*, 893 F.2d 319, 321 (Fed. Cir. 1989) that "claims must be interpreted as broadly as their terms reasonably

allow." Our reviewing court further states that "the words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted).

> Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment.

Superguide Corp. v. DirecTV Enterprises, Inc., 358 F.3d 870, 875 (Fed. Cir. 2004).

> [W]hile an analysis of obviousness always depends on evidence that supports the required Graham factual findings, it also may include recourse to logic, judgment, and common sense available to the person of ordinary skill that do not necessarily require explication in any reference or expert opinion.

Perfect Web Technologies, Inc. v. InfoUSA, Inc., 2009 WL 4281939, at *4 (Fed. Cir. 2009)(Board's emphasis).

ANALYSIS

From our review of the administrative record, we find that the Examiner has presented a prima facie case for the rejections of Appellant's claims under 35 U.S.C. §§ 102(b) and 103(a). The prima facie case is presented on pages 3 to 18 of the Examiner's Answer. In opposition, Appellant presents a number of arguments.

Arguments with respect to the rejection of claims 1, 3 to 5, 8, 10 to 12, 14, 16, 26 to 28, and 31 under 35 U.S.C. § 102(b) [R1]

We select claim 1 as representative. We address the pivotal issue of whether Appellant's claim limitations "synchronously reading the transferred data from all of the two-port memories" and "writing the synchronous read data into the buffer" read on Searby's teachings for simultaneously transferring data (FF#2) and sequentially writing data to the buffer (*id.*), respectively.

Appellant contends:

> [M]erely waiting to collect a full frame of data where the data was already synchronized as it was written into the RAM buffer, as noted above, fails to disclose 'synchronously reading the transferred data from all of the two-port memories, thereby forming synchronous read data, and writing the synchronous read data into the buffer' … as claimed.

(App. Br. 18, middle).

In reply, the Examiner states that Searby's purpose is "to synchronize and buffer image data for parallel and concurrent data transfer." (*See* Abstract; col. 4, ll. 11-28; Ans. 25, top.)

In this case, we note that Appellant argues for a narrower interpretation of "transferred data" than claim 1 requires. (*See* App. Br. 18, middle.) We find unconvincing Appellant's argument that because Searby's data "was already synchronized" (*see* App. Br. 18, middle), Searby fails to meet the claim limitation. Claim 1 merely recites "synchronously reading the transferred data." The "transferred data" of claim 1 is broad claim language, in that the claimed "transferred data" entering the claimed "two-port memories" need not be a particular type of "transferred data." That is,

Appellant's claimed "transferred data" is simply read data (FF#1). Reading the claims broadly but reasonably, *see In re Zletz*, 893 F.2d at 321, we find that Searby meets the limitation because Searby's read data is the same as the "transferred data," as claimed. Since Appellant has not specified that the claimed "transferred data" entering the "two-port memories" is read data of a particular type, Searby's teaching for read data simultaneously transferred to the RAM buffers (Appellant's claimed "two-port memories) meets Appellant's claim limitation "synchronously reading the transferred data" (claim 1).

Regarding the claimed "writing" step of claim 1, Appellant further contends that because data is written sequentially in Searby (as opposed to being written at the same time) from the tri-state buffers 45 to 48 to the data highway 49 and to the register 50 (*see* col. 7, l. 40), the claim limitation "writing the synchronous read data into the buffer" cannot be met by Searby. (*See* Reply Br. 15, top.)

In this case, Appellant argues for a narrower interpretation of "writing" than claim 1 requires (*id.*). We find that the claim does not require synchronously writing (*i.e.*, synchronous transfer of) the claimed "read data." Rather, claim 1 merely recites "writing … read data into the buffer" (claim 1). We remind Appellant that the Board will not read any limitations[2] from the Specification into the claims. (*See Superguide Corp.*, 358 F.3d at 875.) In this case, the claim language (Appellant's claimed "writing") is broader than the embodiment (*i.e.*, synchronously writing or transfer made synchronously, as disclosed in ¶ [0024] of the Specification).

[2] *E.g.*, "The transfer into buffer 52 thus is made synchronously," as disclosed at ¶ [0024] of the Specification.

Since Appellant has not specified that the claimed "writing" is a certain type of writing, Searby's teaching for writing sequentially to the register 50 (Appellant's claimed "buffer") suffices to meet the claim limitation "writing the synchronous read data into the buffer" (claim 1). Accordingly, we find no error.

We address Appellant's contention that Searby fails to teach "receiving and storing read data responsive to timing signals provided by the respective drive," as recited in claim 1 (App. Br. 15, top).

More specifically, Appellant contends that "receiving request signals which control the output of data, as in Searby, does not teach 'causing each of the drives to … transfer the retrieved data from the drive into its corresponding two-port memory using the timing signals provided by the respective drive' … as claimed." (App. Br. 15, bottom).

The Examiner points out in the Answer that Searby teaches Appellant's claimed "causing" step in column 5 at lines 38 to 49 (Ans. 4, middle). Specifically, the Examiner finds that Searby's teaching of a request signal (*i.e.*, "REQ") equates with Appellant's claimed "READ command" (column 5, l. 44; Ans. 4, middle).

We read claim 1 as requiring signals that initiate reads of the disk drives and transfer of read data from the disk drives to two-port memories (FF#1). We find that a skilled artisan would have recognized that Searby's request signals ("REQ"s) are the same as the claimed "timing signals" because Searby teaches sending signals (*i.e.*, "REQ"s or request signals for read commands) that travel between the controller and the disk drives (FF#2), causing each of the drives to transfer read data from the drives into the RAM buffers (*id.*). Regarding the limitation "by the respective drive"

(claim 1), the patent says sub-controllers can be substituted for the single controller to independently monitor request signals and cause read data to be transferred from the SCSI interfaces of the disk stores to the RAM buffers (*id.*). We thus find that the claim limitation "by the respective drive" is indeed met by Searby's alternative teaching for the functionality of the sub-controllers, because the signals to and from Searby's sub-controllers are associated with "each of the respective drives" in the same manner as claimed. In view of Searby's teachings for the request signals ("REQ"s) and the functionality of the sub-controllers, we find unconvincing Appellant's argument that Searby fails to teach the claim limitation "receiving and storing read data responsive to timing signals provided by the respective drive." Accordingly, we find no error.

Appellant further argues: "[W]aiting until all of the disc interfaces have data ready before transferring data, as in Searby, does not teach 'receiving and storing read data responsive to timing signals provided by the respective drive.'" (claim 1) (App. Br. 13, bottom).

We find unconvincing Appellant's argument since the Examiner equated the portion of Searby argued above (*i.e.*, "[W]aiting until all of the disc interfaces have data ready before transferring data") with the claim limitation "waiting until all of the two-port memories indicate such a non-empty condition," and not the claim limitation "receiving and storing read data responsive to timing signals provided by the respective drive." (*See* Ans. 21, top.) Accordingly, we find no error, as both the claim and the Searby reference perform the same "monitoring" function.

Next, Appellant contends:

> Searby's mere disclosure of waiting until all of the disc interfaces have data ready before transferring data fails to meet [A]ppellant's specific claim language, namely 'memory for receiving read data responsive to timing signals provided by the respective drive' in addition to 'synchronously reading the transferred data from all of the … memories.'

(App. Br. 14, middle).

In reply, the Examiner points out that Searby teaches transferring data from the RAM buffers 37 to 40 (Ans. 5, middle).

We carefully considered the Briefs, the Examiner's Answer, both parties' cited portions of Searby, and indeed the entire reference. We agree with the Examiner, in that Searby's data transfer from the RAM buffers meets the claim limitation "synchronously reading the transferred data from all of the two-port memories" for the following reasons.

Words of a claim "are generally given their ordinary and customary meaning." (*See Phillips*, 415 F.3d at 1312.) "The plain meaning of "synchronously" is "happening, arising, or existing at precisely the same time." (*See Webster's New Collegiate Dictionary*, 1182 (1976).) Searby teaches that "[d]ata is output from the RAM buffers 37 to 40 by applying a read strobe signal to the line 54 while simultaneously addressing the same location in each of the stores." (Col. 7, ll. 33-36). Thus, data is called from each of the disc stores (Appellant's claimed "independent disk drives") to the respective RAM buffers (Appellant's claimed "two-port memories") at precisely the same time (*id.*). Further, Searby's words (*i.e.*, data) are sent simultaneously from each of the RAM buffers 37 to 40 to the registers 41 to 44 (*id.* at 33-39).

We read the claim limitation "synchronously reading the transferred data from all of the two-port memories" as being the same as Searby's simultaneously reading data from the same location in each disc store (Appellant's claimed "disk drives") and simultaneously sending the data (Appellant's claimed "transferred data") from the RAM buffers (Appellant's claimed "two-port memories") to the respective registers 41 to 44 (FF#2). Since Searby's data is sent simultaneously to and from the RAM buffers (Appellant's claimed "two-port memories") (FF#2), we find that Searby teaches all that the claim limitation "synchronously reading the transferred data from all of the two-port memories" requires. Reading the claim language broadly but reasonably, *see in re Zletz*, 893 F.2d at 321, we find that Searby's teachings for simultaneously transferring data into and out of the RAM buffers (FF#2) meet Appellant's claim limitation "synchronously reading the transferred data from all of the two-port memories." Accordingly, we decline to find error.

Appellant argues: "[M]erely disclosing controlling means responsive to an indication from a transferring means that data is available for transfer, as in Searby, does not teach 'receiving and storing read data responsive to timing signals provided by the respective drive,' … as claimed." (App. Br. 14, bottom)(emphasis omitted).

We are not persuaded by Appellant's argument concerning Searby's controlling means (App. Br. 14, bottom) because we already addressed above how the Searby reference meets Appellant's claimed "receiving and storing" steps. (*See supra.*) Accordingly, we find no error.

Appellant argues: "[M]erely waiting until all of the disk interfaces have data before transferring data, as in Searby, does not teach

'[transferring] the retrieved data from the drive into its corresponding two-part memory using the timing signals provided by the respective drive,' … as claimed by [A]ppellant." (App. Br. 15, top)(emphasis omitted).

We find unconvincing Appellant's argument since the Examiner equated the portion of Searby argued above (*i.e.*, "[W]aiting until all of the disc interfaces have data ready before transferring data") with the claim limitation "waiting until all of the two-port memories indicate such a non-empty condition," and not "[transferring] the retrieved data from the drive into its corresponding two-part memory using the timing signals provided by the respective drive," as claimed. (*See* Ans. 21, top.) Accordingly, we find no error.

In his own words, Appellant argues: "[Searby] simply fails to even suggest 'monitoring each of the two-port memories to detect a non-empty condition' as claimed." (App. Br. 17, middle)(emphasis omitted).

In reply, the Examiner points out that Searby inherently monitors the RAM buffers for data. (*See* Ans. 4, bottom to Ans. 5, top.) The Examiner reasons that no data will be written from the RAM buffers until all of the RAM buffers contain at least some data *(id.)*.

Words of a claim "are generally given their ordinary and customary meaning." (*See Phillips*, 415 F.3d at 1312.) While we appreciate the Examiner's findings, we need not address inherency, because the plain meanings of Appellant's claimed "monitoring" and Searby's waiting are sufficient to resolve the issue. We find that Appellant's claimed "monitoring" [3] means "to watch, observe, or check especially for a special

[3] As we stated above, the Board will not import any limitations from the Specification, *see Superguide Corp. v. DirecTV Enterprises, Inc.*, cited

purpose." (*See Webster's New Collegiate Dictionary*, 744 (1976).) To wait, as Searby teaches, means to "stay in place in expectation of" (*id.* at 1316). In this case, a skilled artisan would have recognized that Searby's teaching of "waiting" for data to enter the RAM buffers meets Appellant's "claimed" monitoring step, because Searby teaches waiting (FF#2) or staying in place in expectation of data in the same manner that the claimed invention watches, observes or checks (*i.e.*, "monitoring," as claimed) for data. Since Searby's "waiting" and Appellant's claimed "monitoring" are synonymous by their plain meanings, we need not reach the inherency issue and we find that the claim limitation is met. Accordingly, we find no error in the Examiner's analysis of claim 1.

Regarding claim 26, Appellant argues: "[M]erely teaching that data for a requested frame is output from the RAM buffers once it has all been transferred as in Searby, does not teach 'monitoring each of the two-port memories to detect a non-full condition' as claimed." (App. Br. 19, middle)(emphasis omitted).

As we stated above, Appellant's claimed "monitoring" step reads on Searby's waiting for data. (*See supra.*) For the reasons stated above (*see supra*), we find no error in the Examiner's analysis.

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above. Although the Specification discloses at ¶ [0024] that "[s]hould any of the FIFOs become 'empty,' the process will stall until they all indicate 'not empty' once again," the Board will not read this limitation from the Specification into the claims since claim 1 merely requires "waiting until all of the two-port memories indicate such a non-empty condition," as claimed, and not stalling the process once begun.)

Arguments with respect to the rejection of claim 15 under 35 U.S.C. § 103(a) [R2]

> Regarding claim 15, Appellant argues:
>
> [Searby's disclosure] that a register reduces 16-bit words to 8-bit portions, that data is transferred 8 bits at a time, that request signals are generated after 2 bytes of data are received, and that 16-bit words are processed clearly demonstrates that it would not be obvious that 'each synchronous transfer of read data into the common buffer stores 64 bits of read data' … as claimed. . . .
>
> … [T]he Examiner has simply dismissed the same under Official Notice. Appellant … formally requests a specific showing of the subject matter in ALL of the claims in any future action.

(App. Br. 20, middle).

In reply, the Examiner points out that Searby's register (*see* Fig. 2, element 50) stores information 8-bits at a time, instead of the claimed "64-bits." (Ans. 10, bottom). The Examiner takes Official Notice, finding that Searby differs only by the width of the data stored and that such a limitation is merely a design choice that would have been obvious in Searby's system (*id.*).

An obviousness analysis "may include recourse to logic, judgment, and common sense available to the person of ordinary skill that do not necessarily require explication in any reference or expert opinion." *Perfect Web Technologies, Inc. v. InfoUSA, Inc.,* cited above.

We note that the Examiner applies common sense in observing in the Answer that a skilled artisan would have recognized that storing data in 64-bit, 16-bit, or 8-bit increments is commonplace. (*See* Ans. 10, bottom to Ans. 11, top.) That is, the claim limitation "transfer of read data into the

common buffer stores 64-bits of read data" requires only the application of the Examiner's common sense and not a disclosure from a reference. Since our guiding court has held that common sense is a form of recourse available to the Examiner, *see Perfect Web Technologies, Inc.*, cited above, we find unconvincing Appellant's argument that the Examiner must produce a reference that discloses "transfer of read data into the common buffer stores 64-bits of read data," as recited in claim 15. In addition, Appellant has not presented evidence, logic, or precedent to question the force of the Examiner's Official Notice. Thus, in view of the Examiner's Official Notice, the Appellant's lack of support for his challenge and the precedent cited above, we find no error.

Regarding claim 15, Appellant further argues: "[A]t least the third element of the prima facie case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above." (App. Br. 21, middle)(emphasis omitted).

Our guiding court says we are not limited to the *Graham* factors in making a finding of obviousness. (*See Perfect Web Technologies, Inc.*, cited above.) Since we may look beyond the *Graham* factors to the realm of common sense, we will. We thus find unconvincing Appellant's argument regarding the third element of a prima facie case of obviousness because the Examiner's use of common sense is apropos in this instance. Accordingly, we find no error.

Argument with respect to the rejection of claim 6, 7, 13, 29, and 30 under 35 U.S.C. § 103(a) [R3]

Appellant made no arguments regarding the rejection [R3] of claims 6, 7, 13, 29, and 30. Thus, we find no error in the Examiner's analysis.

Arguments with respect to the rejection of claim 2, 9, 17, and 19 to 25 under 35 U.S.C. § 103(a) [R4]

We select claim 17 as representative. Regarding claim 17, Appellant contends: "[M]erely waiting to collect a full frame of video data, where the data was already synchronized as it was written into the RAM buffer, fails to disclose 'synchronously reading data from all of the two-port memories … thereby forming synchronous read data' as claimed." (App. Br. 22, bottom).

Above, we found unconvincing Appellant's argument that because "data was already synchronized" in Searby, the teaching fails to meet the limitation. (*See supra.*) For the above-stated reasons (*see supra*), Searby's teaching meets the claim limitation "synchronously reading transferred data from all of the two-port memories … thereby forming synchronous read data," as claimed. Accordingly, we decline to find error in the Examiner's analysis of claim 17.

Appellant further contends: "[T]he mere disclosure that the word is output as each tri-state buffer is enabled in sequence and individually output from the register to the highway, as in Searby, simply fails to even suggest 'forming synchronous read data' by 'synchronously reading data from all of the two-port memories' as claimed." (App. Br. 23, middle)(emphasis omitted).

As we stated above (*see supra*), Appellant's argued limitations do indeed read on Searby's teachings for data written sequentially to the register 50 (FF#2). For the same reasons stated above (*see supra*), Searby's teachings meet Appellant's claim limitations "forming synchronous read data" and "synchronously reading transferred data from all of the two-port memories." Accordingly, we find no error in the Examiner's analysis of claim 17.

Argument with respect to the rejection of claim 18 under 35 U.S.C. § 103(a) [R5]

Appellant made no arguments regarding the rejection [R5] of claim 18. Thus, we find no error in the Examiner's analysis.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 1-31.

DECISION

We affirm the Examiner's rejection of claims 1-31.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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ZILKA-KOTAB, PC
P.O. BOX 721120
SAN JOSE, CA 95172-1120